## **Power MOSFET**

# 30 V, 94 A, Single N-Channel, SOIC-8 FL

### **Features**

- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These are Pb-Free Devices

## **Applications**

- VCORE Applications
- DC-DC Converters
- Low Side Switching

## MAXIMUM RATINGS (T<sub>.1</sub>=25°C unless otherwise stated)

	. •				
Ra	ating		Symbol	Value	Unit
Drain-to-Source Vo	Itage		$V_{DSS}$	30	V
Gate-to-Source Vol	tage		$V_{GS}$	±20	V
Continuous Drain Current R <sub>0.IA</sub>		T <sub>A</sub> = 25°C	I <sub>D</sub>	18	Α
(Note 1)		T <sub>A</sub> = 85°C		13	
Power Dissipation R <sub>θJA</sub> (Note 1)		T <sub>A</sub> = 25°C	P <sub>D</sub>	2.35	W
Continuous Drain Current R <sub>BJA</sub>		T <sub>A</sub> = 25°C	Ι <sub>D</sub>	11	Α
(Note 2)	Steady State	T <sub>A</sub> = 85°C		8.0	
Power Dissipation R <sub>θJA</sub> (Note 2)	Sidle	T <sub>A</sub> = 25°C	$P_{D}$	0.91	W
Continuous Drain Current R <sub>BJC</sub>		T <sub>C</sub> = 25°C	Ι <sub>D</sub>	94	Α
(Note 1)		T <sub>C</sub> = 85°C		68	
Power Dissipation R <sub>θJC</sub> (Note 1)		T <sub>C</sub> = 25°C	P <sub>D</sub>	62.5	W
Pulsed Drain Cur- rent		= 25°C, : 10 μs	I <sub>DM</sub>	140	Α
Current limited by package	T <sub>A</sub> :	= 25°C	I <sub>DmaxPkg</sub>	140	Α
Operating Junction a Storage Tempera			T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C
Source Current (Boo	dy Diode)		I <sub>S</sub>	62.5	Α
Drain to Source			dV/dt	10	V/ns
	to-Source Avalanche $_{\rm DD}$ = 50 V, $_{\rm GS}$ = 10 V, $_{\rm MH}$ , $_{\rm G}$ = 25 $_{\rm MH}$		E <sub>AS</sub>	450	mJ
Lead Temperature for (1/8" from case for		g Purposes	TL	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

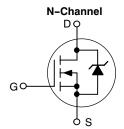
- 1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
- 2. Surface-mounted on FR4 board using the minimum recommended pad size.



## ON Semiconductor®

## http://onsemi.com

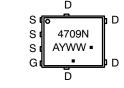
V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> Typ	I <sub>D</sub> Max	
30 V	2.85 m $\Omega$ @ 10 V	94 A	
30 V	4.0 mΩ @ 4.5 V	5 <del>4</del> A	





STYLE 1

# MARKING DIAGRAM & PIN ASSIGNMENT



4709N = Specific Device Code A = Assembly Location

Y = Year WW = Work Week • Pb-Free Package

(Note: Microdot may be in either location)

## **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NTMFS4709NT1G	SOIC-8 FL (Pb-Free)	1500 / Tape & Reel
NTMFS4709NT3G	SOIC-8 FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## THERMAL RESISTANCE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{ hetaJC}$	2.0	°C/W
Junction-to-Ambient - Steady State (Note 3)	$R_{ hetaJA}$	53.2	
Junction-to-Ambient - Steady State (Note 4)	$R_{ hetaJA}$	137.8	

## **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	•						•
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>I</sub>	<sub>D</sub> = 250 μA	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T				5.6		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V,	T <sub>J</sub> = 25°C			1.0	μΑ
		V <sub>DS</sub> = 24 V	T <sub>J</sub> = 125°C			10	1
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V	GS = ±20 V			±100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}$ , I	D = 250 μA	1.0		3.0	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>				5.6		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 11.5 V	I <sub>D</sub> = 30 A		2.8		
			I <sub>D</sub> = 15 A		2.8		
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A		2.85	3.6	mΩ
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 30 A		4.0	5.5	
			I <sub>D</sub> = 15 A		4.0		
Forward Transconductance	9FS	V <sub>DS</sub> = 15 V,	, I <sub>D</sub> = 15 A		41		S
CHARGES AND CAPACITANCES							
Input Capacitance	C <sub>ISS</sub>				2370		
Output Capacitance	C <sub>OSS</sub>	$V_{GS} = 0 \text{ V, f} = 1 \text{ MHz,}$ $V_{DS} = 12 \text{ V}$			1240		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>				305		
Total Gate Charge	Q <sub>G(TOT)</sub>				20		
Threshold Gate Charge	Q <sub>G(TH)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 15 V; I <sub>D</sub> = 30 A			2.4		nC
Gate-to-Source Charge	$Q_{GS}$				4.5		
Gate-to-Drain Charge	$Q_{GD}$				11		
Total Gate Charge	Q <sub>G(TOT)</sub>				48		
Threshold Gate Charge	Q <sub>G(TH)</sub>	V <sub>GS</sub> = 11.5 V, V <sub>DS</sub> = 15 V; I <sub>D</sub> = 30 A			4.0		nC
Gate-to-Source Charge	$Q_{GS}$				6.5		
Gate-to-Drain Charge	$Q_{GD}$				10.6		
OWITOUING QUADACTERISTICS (Notes of	•						-
SWITCHING CHARACTERISTICS (Note 6)							
Turn-On Delay Time	t <sub>d(ON)</sub>				16		
	t <sub>d</sub> (ON)	V <sub>GS</sub> = 4.5 V V	Vns = 15 V.		16 173		
Turn-On Delay Time		V <sub>GS</sub> = 4.5 V, V <sub>ID</sub> = 30 A, F	$V_{DS} = 15 \text{ V},$ $R_{G} = 3.0 \Omega$				ns

<sup>5.</sup> Pulse Test: pulse width  $\pm\,300~\mu\text{s},$  duty cycle  $\pm\,2\%$ 

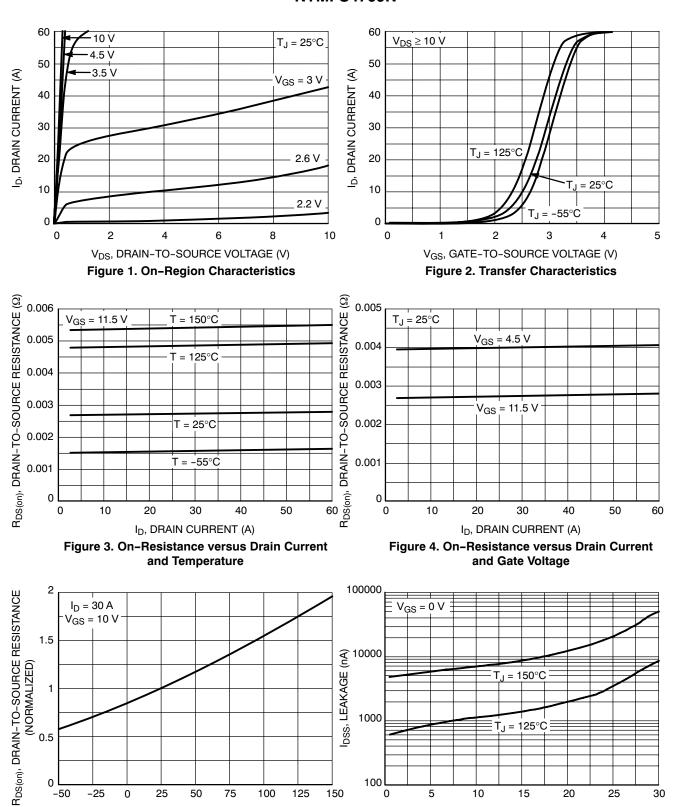
Surface-mounted on FR4 board using 1 sq in pad, 1 oz Cu.
 Surface-mounted on FR4 board using the minimum recommended pad size.

<sup>6.</sup> Switching characteristics are independent of operating junction temperatures.

# **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
SWITCHING CHARACTERISTICS (Note	e 6)	•			•		•
Turn-On Delay Time	t <sub>d(ON)</sub>				8.5		
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 11.5 V	, V <sub>DS</sub> = 15 V,		87		ns
Turn-Off Delay Time	t <sub>d(OFF)</sub>	V <sub>GS</sub> = 11.5 V I <sub>D</sub> = 30 A, I	$R_{\rm G} = 3.0  \Omega$		31.5		
Fall Time	t <sub>f</sub>	1			8.5		1
DRAIN-SOURCE DIODE CHARACTER	ISTICS						
Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 20 A	T <sub>J</sub> = 25°C		0.75	1.0	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 50 A	T <sub>J</sub> = 25°C		0.85		
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 20 A	T <sub>J</sub> = 125°C		0.7		
Reverse Recovery Time	t <sub>RR</sub>		•		48		
Charge Time	ta	$V_{GS} = 0 \text{ V},$ $d_{IS}/d_t = 100 \text{ A}/\mu\text{s},$ $I_S = 25 \text{ A}$			23		ns
Discharge Time	t <sub>b</sub>				25		
Reverse Recovery Charge	Q <sub>RR</sub>				55		nC
Package Parasitic Values	•				•	•	•
Gate Resistance	$R_{G}$	T <sub>A</sub> = 25°C			0.65		Ω

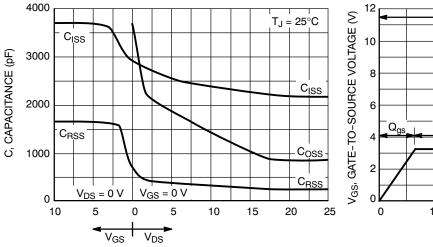
<sup>5.</sup> Pulse Test: pulse width  $\pm 300~\mu s$ , duty cycle  $\pm 2\%$ 6. Switching characteristics are independent of operating junction temperatures.



T<sub>J</sub>, TEMPERATURE (°C)
Figure 5. On–Resistance Variation with
Temperature

V<sub>DS</sub>, DRAIN-TO-SOURCE VOLTAGE (V)

Figure 6. Drain-to-Source Leakage Current versus Voltage



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (V)

Figure 7. Capacitance Variation

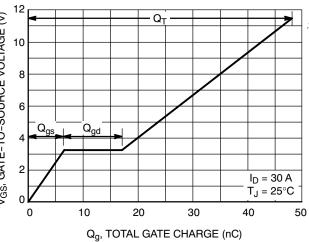


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

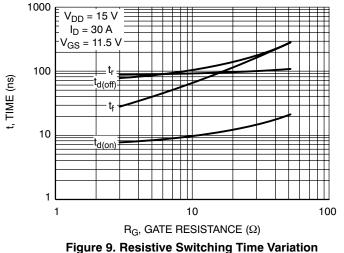


Figure 9. Resistive Switching Time Variation versus Gate Resistance

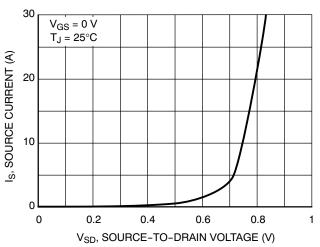
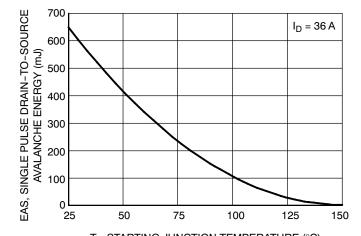


Figure 10. Diode Forward Voltage versus Current

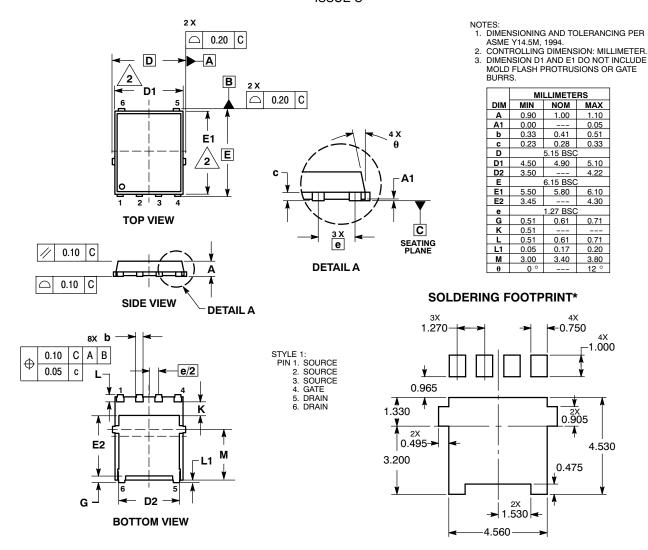


TJ, STARTING JUNCTION TEMPERATURE (°C)

Figure 11. Maximum Avalanche Energy versus Starting Junction Temperature

#### PACKAGE DIMENSIONS

## DFN6 5x6, 1.27P (SO8 FL) CASE 488AA-01 ISSUE C



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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